Docket No.: 50006-128 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	Customer Number: 20277
Makoto NAGATA, et al.	Confirmation Number: 4496
Serial No.: 09/977,994	Group Art Unit: 2857
Filed: October 17, 2001	Examiner: West, Jeffrey R

For: METHOD AND APPARATUS FOR ANALYZING A SOURCE CURRENT WAVEFORM IN A SEMICONDUCTOR INTEGRATED CIRCUIT

DECLARATION UNDER 37 CFR 1.132

Mail Stop Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Makoto Nagata, hereby declare and say as follows:

1. That I am an inventor named in this patent application Serial No. 09/977,994 (hereinafter the "'994 application").

2. That I am familiar with the prosecution of this application and understand that the claims of the application stand rejected on the various grounds citing at least Nagata et al., "Measurements and Analyses of Substrate Noise Waveform in Mixed Signal IC Environment," in view of Nagata et al., "Physical Design Guides for Substrate Noise Reduction in CMOS Digital Circuits" (hereinafter "Nagata CMOS"). It is also my understanding that the Examiner cited Nagata CMOS to identify subject matter which was disclosed at the Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, held in Florida, U.S., in May of 2000 (hereinafter the "IEEE Conference"). It is further my understanding that this subject matter on

which the Examiner relies corresponds to disclosure of the '994 application relating to representing a digital circuit and generating an analysis model in accordance with a time-division group of parasitic capacitors.

3. That I have knowledge of the subject matter disclosed at the IEEE Conference. To the best of my recollection and knowledge, the subject matter of Nagata CMOS on which the Examiner relies was not disclosed or disseminated in any manner during the IEEE Conference. To the best of my knowledge, this subject matter was first publicly disclosed in the Nagata CMOS article, which was published in March 2001 and within one year of the U.S. filing date, as identified above.

4. That, to the best of my recollection and knowledge, the document entitled "Proceedings of the IEEE 2000 Custom Integrated Circuits Conference" and accompanying article entitled "Quantitative Characterization of Substrate Noise for Physical Design Guides in Digital Circuits" identifies subject matter that was disclosed at the IEEE conference.

5. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Respectfully submitted,

2004. 1. 21
Date

Makoto Nagata